What is claimed is:

[Claim 1] 1. A field effect transistor (FET) comprising:

a fin structure;

conducting spacers positioned adjacent to said fin structure;

an insulator adjacent to said spacers; and

a gate layer positioned on said fin structure, said spacers, and said insulator.

[Claim 2] 2. The FET of claim 1, further comprising:

a substrate; and

an isolation layer positioned over said substrate,

wherein said isolation layer is positioned under said insulator, said spacers, and said fin structure.

[Claim 3] 3. The FET of claim 2, further comprising source/drain regions above said isolation layer.

[Claim 4] 4. The FET of claim 1, wherein said fin structure comprises an oxide layer over a silicon layer.

[Claim 5] 5. The FET of claim 1, further comprising an oxide layer adjacent to said fin structure.

[Claim 6] 6. The FET of claim 4, further comprising a second oxide layer over said oxide layer, wherein said second oxide layer is planar to said gate layer.

[Claim 7] 7. The FET of claim 1, wherein said spacers and said gate layer comprise the same material.

[Claim 8] 8. The FET of claim 7, wherein said material comprises polysilicon.

[Claim 9] 9. The FET of claim 1, further comprising a gate insulator positioned between said fin structure and said spacers.

[Claim 10] 10. The FET of claim 1, further comprising a second insulator adjacent to said insulator.

[Claim 11] 11. A field effect transistor (FET) device comprising:

a fin structure;

a first gate electrode adjacent to said fin structure;

a gate insulator positioned between said first gate electrode and said fin structure;

a second gate electrode positioned transverse to said first gate electrode; and

a third gate electrode positioned on said fin structure, said first gate electrode, and said second gate electrode.

[Claim 12] 12. The device of claim 11, further comprising:

a substrate; and

an isolation layer positioned over said substrate,

wherein said isolation layer is positioned beneath said gate insulator, said first gate electrode, and said fin structure.

[Claim 13] 13. The device of claim 12, wherein said isolation layer is isolated from said second gate electrode.

[Claim 14] 14. The device of claim 12, further comprising source/drain regions above said isolation layer.

[Claim 15] 15. The device of claim 11, further comprising a dielectric material sandwiching said second gate electrode.

[Claim 16] 16. The device of claim 11, wherein said fin structure comprises an oxide layer over a silicon layer.

[Claim 17] 17. The device of claim 11, further comprising an oxide layer adjacent to said fin structure.

[Claim 18] 18. The device of claim 16, further comprising a second oxide layer over said oxide layer, wherein said second oxide layer is planar to said third gate electrode.

[Claim 19] 19. The device of claim 11, wherein said first gate electrode and said third gate electrode comprise the same material.

[Claim 20] 20. The device of claim 19, wherein said material comprises polysilicon.

[Claim 21] 21. A method of lowering a gate capacitance and extrinsic resistance in a field effect transistor (FET), said method comprising:

forming a fin structure;

configuring a first gate electrode adjacent to said fin structure;

disposing a gate insulator between said first gate electrode and said fin structure;

positioning a second gate electrode transverse to said first gate electrode; and

depositing a third gate electrode on said fin structure, said first gate electrode, and said second gate electrode.

[Claim 22] 22. The method of claim 21, further comprising forming an isolation layer over a substrate, wherein said isolation layer comprises a buried oxide (BOX) layer, and wherein said isolation layer is positioned beneath said gate insulator, said first gate electrode, and said fin structure.

[Claim 23] 23. The method of claim 22, further comprising configuring source/drain regions above said isolation layer.

[Claim 24] 24. The method of claim 21, further comprising sandwiching said second gate electrode with a dielectric material.

[Claim 25] 25. The method of claim 21, wherein said fin structure is formed by depositing an oxide layer over a silicon layer.

[Claim 26] 26. The method of claim 21, further comprising forming an oxide layer adjacent to said fin structure.

[Claim 27] 27. The method of claim 25, further comprising forming a second oxide layer over said oxide layer, wherein said second oxide layer is planar to said third gate electrode.

[Claim 28] 28. The method of claim 21, further comprising using the same material to form said first gate electrode and said third gate electrode.

[Claim 29] 29. The method of claim 28, wherein said material comprises polysilicon.